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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/517,345	03/02/00	ANDERSON S	15114-052310

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EXAMINER	
PAREKH, N	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/26/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/517,345	Anderson et al
Examiner	**Group Art Unit**
Nitin Parekh	2811

☒ Responsive to communication(s) filed on *Jul 14, 1900*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-25* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-25* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art (cited IDS reference-Schueller) in view of Solberg (US Pat. 6054337).

Regarding claims 1 and 18, the cited prior art discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die having a first thickness
- a metallized polymer layer having a first side and a second side, and
- a transition medium/support structure disposed between the silicon die and the first side of the metallized polymer layer where the transition medium/support structure has a second thickness (Fig. 3B; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

The prior art fails to specify the first thickness of the silicon die being less than the second thickness. Solberg teaches using a silicon die with a smaller thickness than that of a transition medium/compliant element in a tape carrier/IC package (Fig. 10; Fig. 6-10; Col. 9, line 35- Col.

10, line 60). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the first thickness of the silicon die with a smaller thickness than the second thickness of transition medium to reduce the thermal stress using Solberg's design in the prior art as cited in claims 1 and 18.

Regarding claim 2, the prior art discloses the transition medium/support structure of conventional nonconductive epoxy type material (Col. 10, line 18-27).

Regarding claim 3, the prior art discloses encapsulating the silicon die and the transition medium with a conventional plastic encapsulant/mold cap (Col. 8, line 40; Fig. 3B). The conventional encapsulant and adhesives have thermal coefficient of expansion (TCE) range of 7-15 x $10^{-6}/^{0}$C and approximately 58 x $10^{-6}/^{0}$C respectively (Table 2- admitted prior art). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate a plastic encapsulant having approximate TCE range of 7-17 x $10^{-6}/^{0}$C to reduce the thermal stress in the prior art in view of Solberg as cited in claim 1.

Regarding claims 4 and 5, the prior art discloses the transition medium/support structure used to reduce the thermal stress/ cracks and to improve the reliability and of conventional nonconductive epoxy/PCB type material (Col. 10, line 18-27) but fails to specify the range of TCE of the material. The prior art further discloses conventional BGA packages using elastomers

and adhesives as a transition medium (Fig. 2; Col. 5 and 6) to reduce the thermal stress. It is conventional in chip packaging art to use such nonconductive material/packaging substrates as epoxy, molded plastic, FR-4/5, BT resin, etc. which have typical TCE in the range of 10-17 x $10^{-6}/^{0}C$. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the transition medium comprising molded compound, FR-4/5, or BT resin compound and having the TCE range of 7-17 x $10^{-6}/^{0}C$ to reduce the thermal stress in the prior art in view of Solberg as cited in claims 4 and 5.

Claim 6 is rejected as explained above for claims 4 and 5.

Claim 7 is rejected as explained above for claim 1.

Regarding claims 8, 9, 16 and 17, the prior art fails to specify the dimensions such as the thickness of the package and die or the cross-sectional area of the die being larger than that of the transition medium. However, in the chip packaging art, such parameters as the package/die thickness, area, area ratio of various components, volume, weight, etc. are considered to be a matter of design choice and are selected to meet device performance and reliability requirements. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the thickness of the package and the die to be less than approximately 0.060 inches and 6 mils respectively and the area of the die being less than, equal

or larger than that of the transition medium to meet the design requirements in the prior art in view of Solberg as cited in claims 8, 9, 16 and 17 respectively.

Regarding claim 10, the prior art discloses coupling of the silicon die to the transition medium using an adhesive (Fig. 3B; Layer 64).

Claim 11 is rejected as explained above for claim 3.

Regarding claims 12-15, the prior art discloses a tape carrier having a dielectric and conductive layers as IC metallized polymer layer and solder balls mounted to the second side of the metallized polymer layer, the solder balls electrically contacting the etched circuit in a conductive layer of the tape carrier and arranged in a grid fashion under the position of the die and connecting the package to a PCB (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

Claim 19 is rejected as explained above for claims 8, 9, 16 and 17.

Claim 20 is rejected as explained above for claims 1 and 3.

Claim 21 is rejected as explained above for claims 20 and 1-5.

Claim 22 is rejected as explained above for claims 20, 1 and 10.

Claim 23 is rejected as explained above for claims 20, 1, 2 and 4.

Claim 24 is rejected as explained above for claims 20, 1 and 12.

Claim 25 is rejected as explained above for claims 1-19 and 20-24 and as further disclosed (prior art) using the first and second adhesive layers having a TCE disposed on the tape carrier and the transition medium respectively (Fig. 3B; Col. 9, line 65; Col. 8, line 12- Col. 10, line 36).

Papers related to this application may be submitted directly to Art Unit 2811 by Facsimile transmission. Papers should be faxed to Art Unit via Tech Center 2800 fax center located in Crystal Plaza 4, Room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh at (703) 305-3410. The examiner can normally be reached on Monday-Friday from 08:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh (09-19-00)

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER